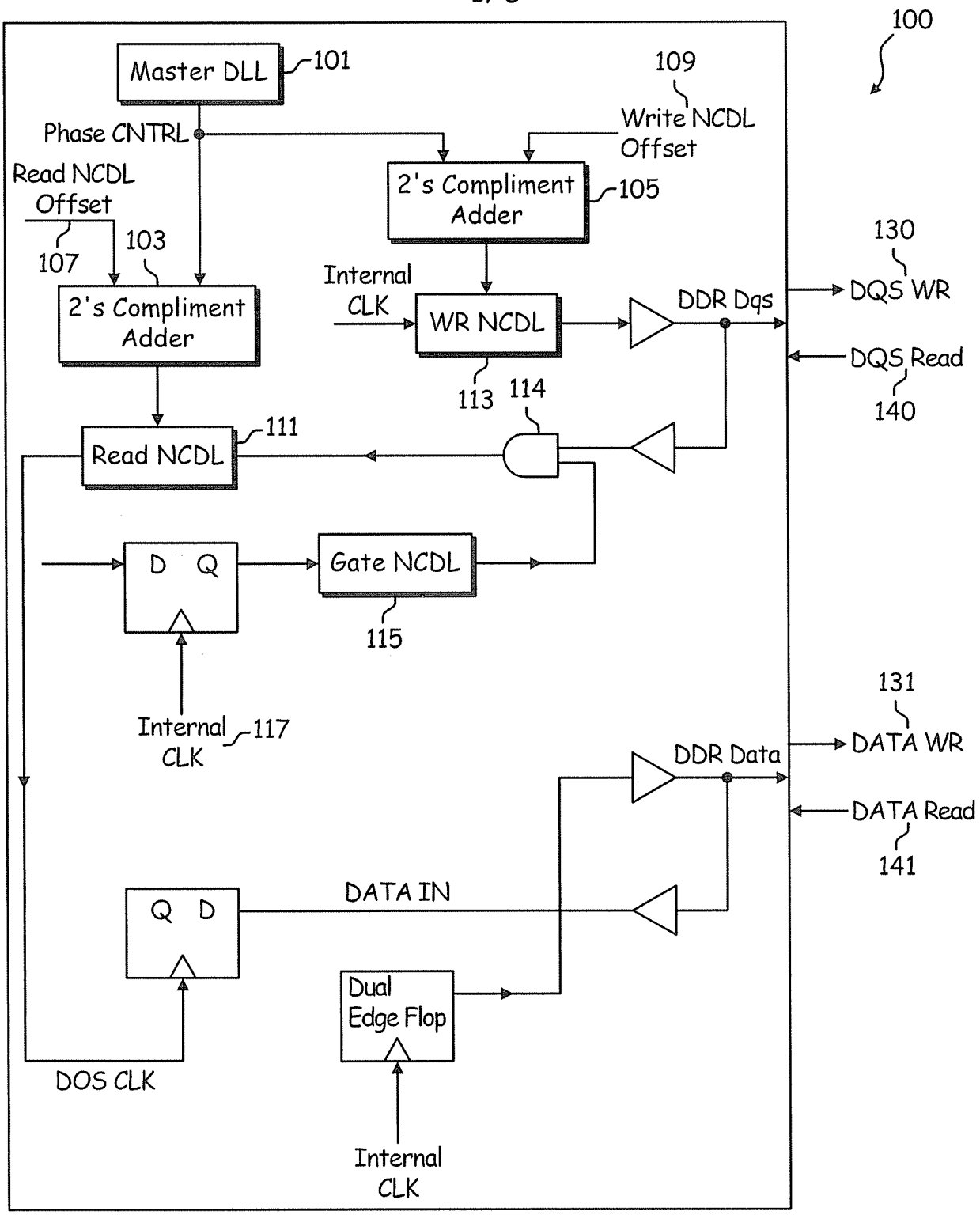
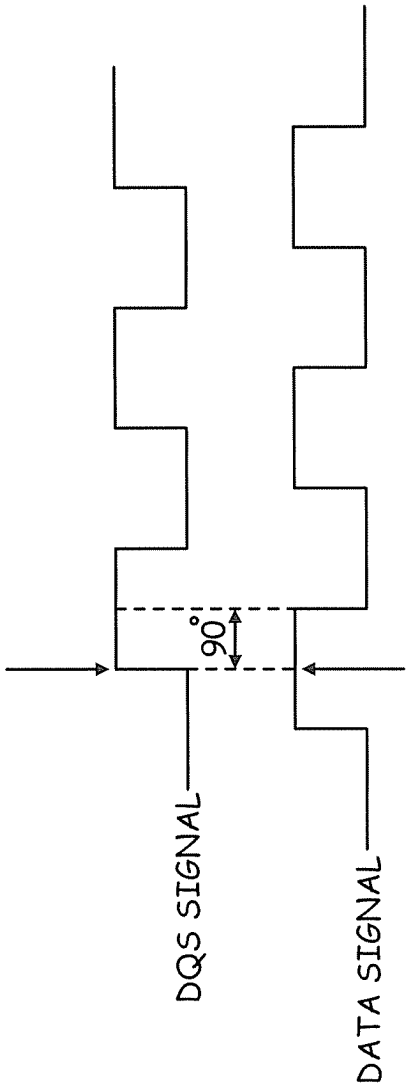


DLL and NCDL Mechanism in DDR Memory Controller

FIG. 1A



CENTER ALIGNMENT OF DQS AND DATA SIGNALS

FIG. 1B

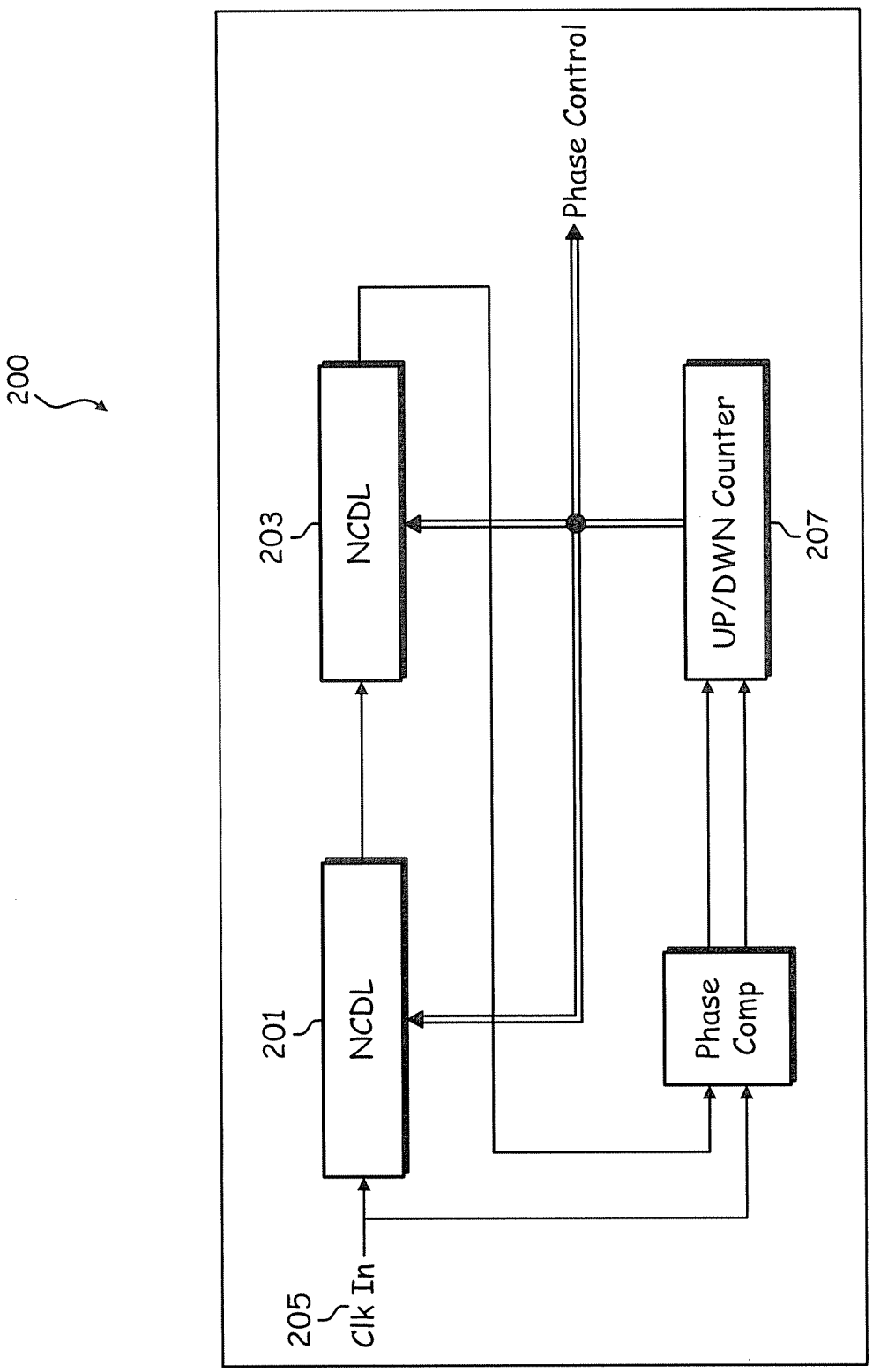

200
Phase Control
203
NCDL
207
UP/DWN Counter
201
NCDL
Phase Comp
205
Clk In
Delay Locked Loop

FIG. 2

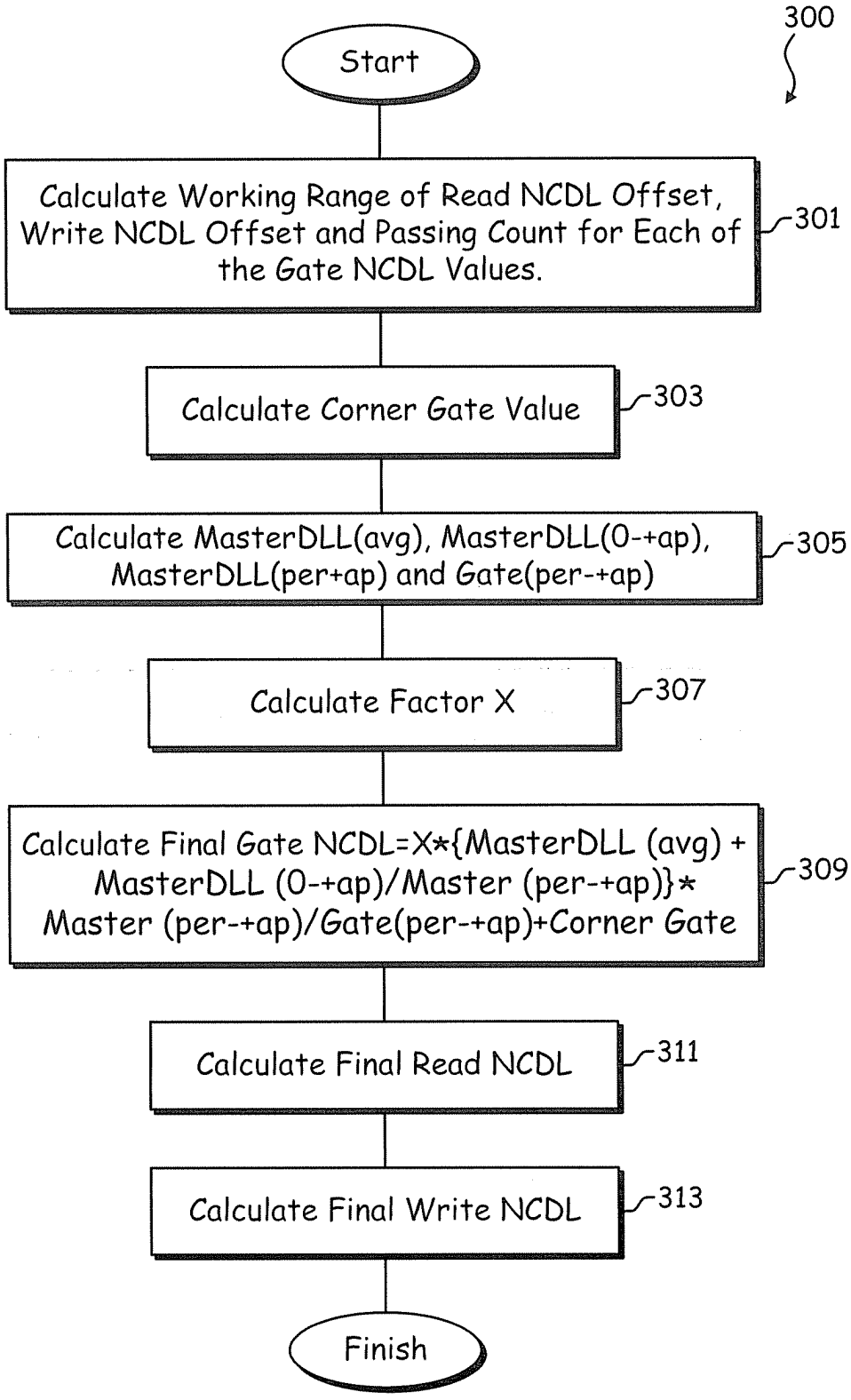
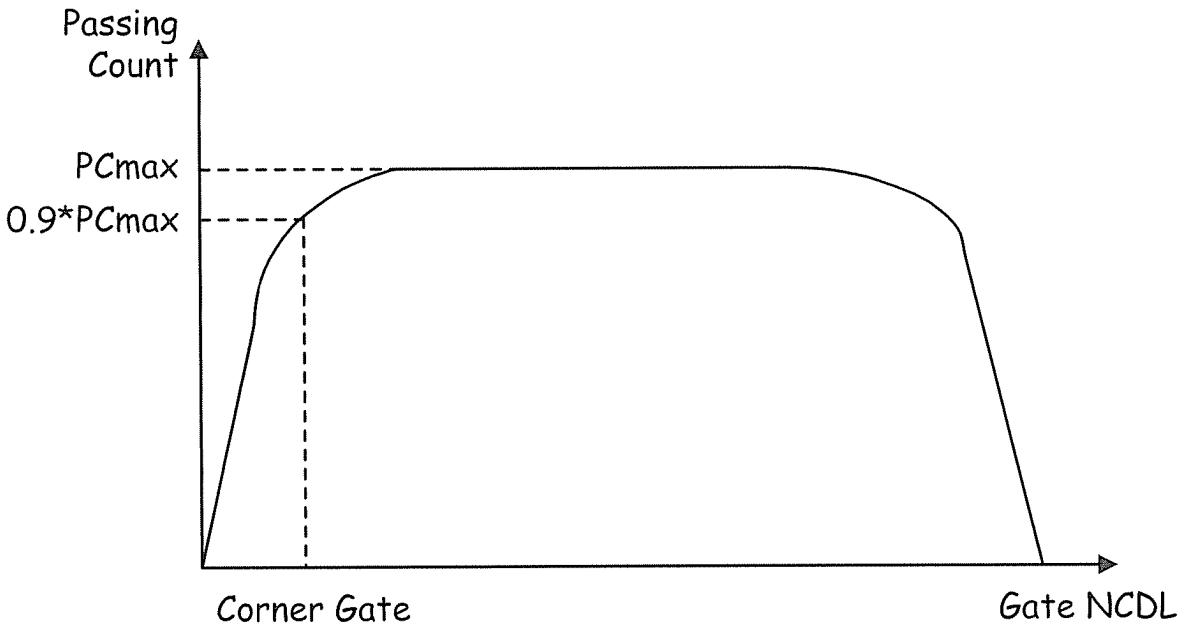

300
Start
Calculate Working Range of Read NCDL Offset, Write NCDL Offset and Passing Count for Each of the Gate NCDL Values.
301
Calculate Corner Gate Value
303
Calculate MasterDLL(avg), MasterDLL(0-+ap), MasterDLL(per+ap) and Gate(per-+ap)
305
Calculate Factor X
307
Calculate Final Gate NCDL=X*{MasterDLL (avg) + MasterDLL (0-+ap)/Master (per-+ap)}* Master (per-+ap)/Gate(per-+ap)+Corner Gate
309
Calculate Final Read NCDL
311
Calculate Final Write NCDL
313
Finish

FIG. 3



Plot of Passing Count Vs Gate NCDL

FIG. 4

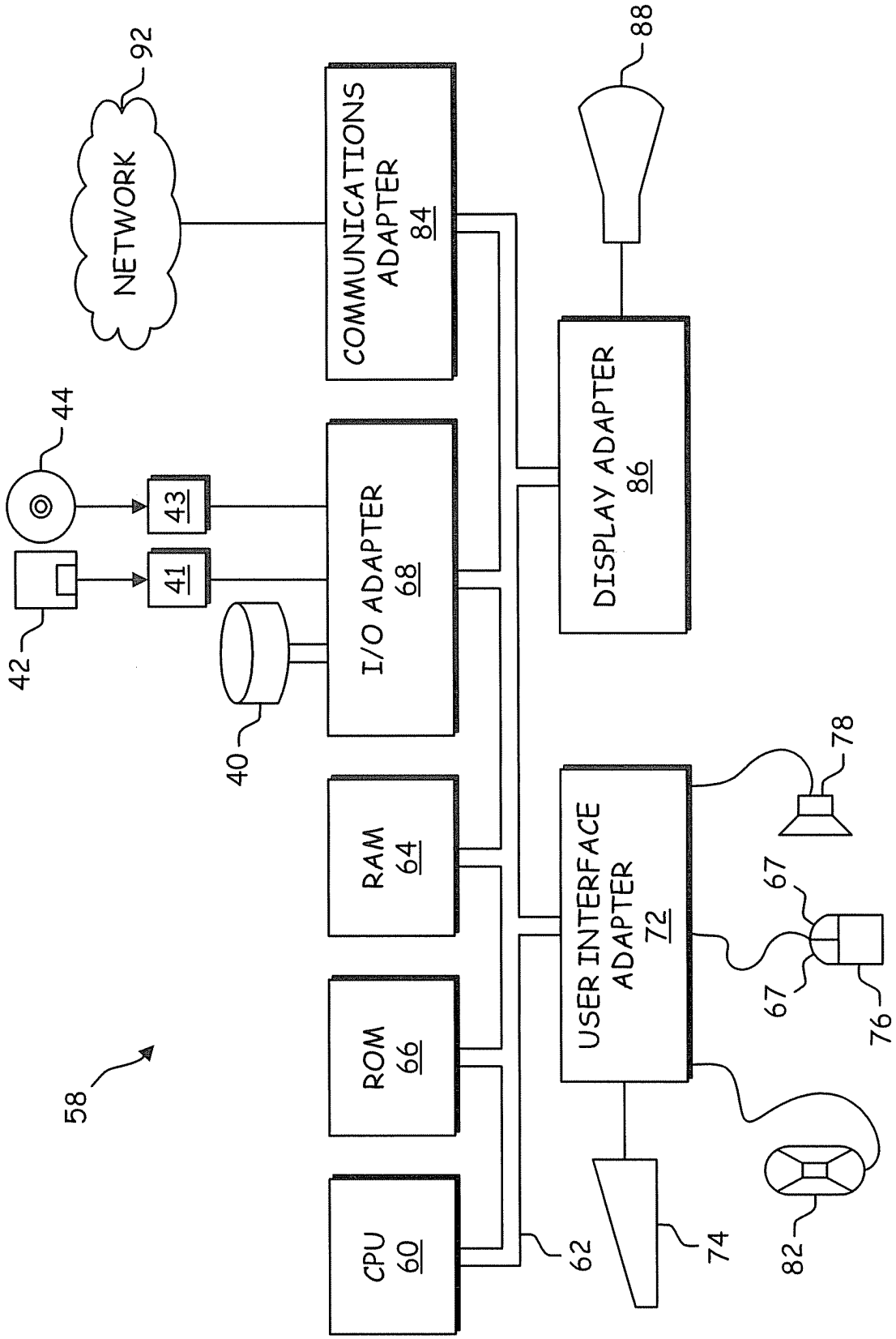

58
CPU 60
ROM 66
RAM 64
I/O ADAPTER 68
COMMUNICATIONS ADAPTER 84
NETWORK
92
DISPLAY ADAPTER 86
88
USER INTERFACE ADAPTER 72
62
74
82
78
67
67
76
40
42
41
43
44

FIG. 5